36V, 10A Step-Down Switching Regulator

1 Features

- 4.5V to 36V wide operating input range
- 10A continuous output current capability
- Dynamical programming of output current and Output voltage using PWM signal or analog signal
- Adjustable Switching Frequency using resistor
- Frequency dithering for good EMI performance
- Integrated 2-A MOSFET Gate Drivers
- Comprehensive protection features including Output Short Protection (OSP), Cycle-by-Cycle input and output Peak Current Limit, thermal regulation, thermal shutdown, input UVLO, input OVP, output OVP etc.
- Output Average Current Limiting with stable CC loop
- 5V/55mA low I_q LDO to power system MCU
- QFN4x4-20 Package

2 Applications

- Automotive Start-Stop Systems
- Industrial PC Power Supplies
- USB Power Delivery

3 Description

PL56001 is a PWM controller, designed for high performance synchronous Buck DC/DC applications with input voltages 4.5 V to 32 V (36 V maximum).

PL56001 employs Constant ON time control. The switching frequency could be set to 150kHz, 300kHz, 600kHz or 1200kHz based on different resistor value between FREQ pin and GND pin. The device also features a programmable soft-start function and offers all kinds of protection features including cycle-by-cycle current limiting, input under voltage lockout (UVLO), output over voltage protection (OVP), input Over Voltage Protection, thermal shutdown and output short protection etc.

PL56001 provides voltage control loop, constant current loop, and thermal regulation loop.

4 Typical Application Schematic

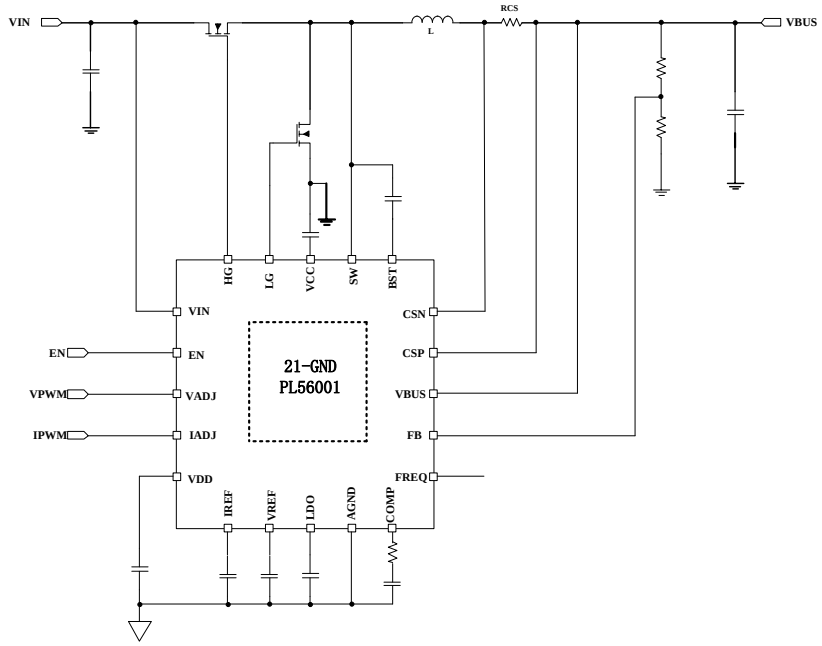


Fig. 1 Application Schematic

5 Pin Configuration and Functions

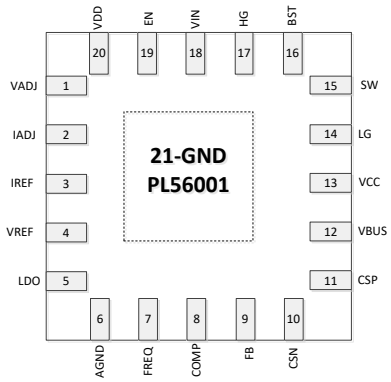


Fig. 2 Pin-Function (QFN4X4-20)

Pin		Description
Number	Name	
1	VADJ	Connect a 0-2V analog voltage or a PWM signal to program voltage reference on VREF pin. Connect this pin to VDD will force VREF to constant 2V.
2	IADJ	Connect a 0-2V analog voltage or a PWM signal to program voltage reference on IREF pin. Connect this pin to VDD will force IREF to 2V.
3	IREF	Reference voltage for input and output current limiting loop.
4	VREF	Voltage reference for voltage control loop
5	LDO	Low quiescent current 5V/55mA LDO. Directly powered from VIN pin. LDO can be used as power supply for application processor such as MCU. When EN is low, only this LDO will be active to power MCU and keep low quiescent current for the whole system.
6	AGND	
7	FREQ	Connect to GND to set the switching frequency at 150kHz. Connect this pin to VDD to set switching frequency at 300kHz. Connect to a resistor divider between VDD and GND to set frequency to 600k and 1200k Hz.
8	COMP	Error Amplifier output.
9	FB	VBUS voltage feedback. Connect a resistor divider between VBUS and GND to FB to program VBUS voltage in battery discharging mode.
10	CSN	he minus input of output current sense.
11	CSP	The positive input of output current sense.
12	VBUS	VBUS voltage
13	VCC	6.6V power supply for high side and low side driver
14	LG	Low side MOSFET driver output.
15	SW	Connect this pin to the Switching point of the power stage.
16	BST	Boost pin for high side MOSFET driver.
17	HG	High side MOSFET driver.
18	VIN	Input voltage.
19	EN	Logic High will enable the converter. Logic Low will disable the whole PL56001 except LDO. Only LDO is working to power system MCU when EN is low. EN is pulled high internally by a high value resistor.
20	VDD	5.4V power supply for PL56001 control core.

6 Device Marking Information

Part Number	Order Information	Package	Package Qty	Top Marking
PL56001	**PL56001IQN20**	**QFN4x4 - 20**	**4000**	**56001 RAAYMD**

PL56001: Part Number
RAAYMD: RAA: LOT NO.; YMD: Package Date

7 Specifications

7.1 Absolute Maximum Ratings(Note1)

PARAMETER	MIN	MAX	Unit
VIN, VBUS, CSN, CSP, SW	-0.3	40	V
HG, BST to SW	-0.3	7	
LG, VCC to GND	-0.3	7	
CSP to CSN	-0.3	0.6	
VBUS to CSP, CSN	-0.3	0.6	
Other Pins to GND	-0.3	6	

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
T_{ST}	Storage Temperature Range	-65	150	°C
T_J	Junction Temperature		+150	°C
T_L	Lead Temperature		+260	°C
V_{ESD}	HBM Human body model	2		kV

7.3 Recommended Operating Conditions (Note 2)

	PARAMETER	MIN	MAX	Unit
Input Voltages	VIN，VBUS	3.6	32	V
Temperature	Operating junction temperature range, T_J	-40	+125	°C

7.4 Thermal Information(Note 3)

Symbol	Description	QFN4X4-32	Unit
θ_{JA}	Junction to ambient thermal resistance	44	°C/W
θ_{JC}	Junction to case thermal resistance	9	

Notes:
1) Exceeding these ratings may damage the device.
2) The device function is not guaranteed outside of the recommended operating conditions.
3) Measured on approximately 1" square of 1 oz copper.

7.5 Electrical Characteristics (Typical at VIN = 12V, T_J =25°C, unless otherwise noted.)

Supply voltages	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
VIN	Input voltage		4.5		32	V
$I_{Q\_}$ VIN	VIN Shutdown Current	EN=0V, VIN=7.2V		15		uA
	VIN Supply Current	No Switching, FB=2.1V		1000		uA
VBUS	Bus line voltage		2		30	V
$I_{Q_}$VBUS	VBUS Shutdown Current	EN=0V, VBUS=7.2V		15		uA
	VBUS Supply Current	No Switching, battery fully charged		1200		uA
V_{VCC}	Driver power supply voltage	VIN =15V		6.6		V
V_{VDD}	Control core power supply voltage	VIN =15V		5.4		V
V_{LDO}	LDO output voltage	VIN =15V		5		V
I_{LDO}	LDO output current	V_{LDO} =5V			55	mA
UVLO/EN						
$VIN_{\_UV}$	VIN UVLO Rising			3.5		V
	UVLO Hysteresis			300		mV
$VBUS_{\_UV}$	VBUS UVLO Rising			3.5		V
	UVLO Hysteresis			300		mV
V_{EN_UV}	Operation Threshold		1.1	1.2	1.3	V
	Hysteresis			200		mV
VREF						
V_{VREF_Dischg}	VREF voltage in discharge mode	VADJ connected to VDD		2		V
V_{VREF_chg}	VREF voltage in charge mode	VADJ connected to VDD		1.8		V
Control loop						
V_{FB}	VFB regulation voltage in discharging mode	FB voltage		2		V
D_{max}	Maximum Duty Cycle(Note 4)				92	%
G_{mEA}	Error amplifier gm			450		uS
I_{SINK}	COMP sink/source current	VFB=VREF+100mV		15		uA
I_{SOURCE}	COMP source current	VFB=VREF-100mV		20		uA
I_{FB}	FB bias current	FB2 in regulation			100	nA
Frequency						
F_{SW}	Switching Frequency	FREQ 0-0.4V, short FREQ pin to GND.		150		KHz
		FREQ 1.8-5.4V, short FREQ pin to VDD.		300		KHz
		FREQ 0.4-0.85V		600		KHZ
		FREQ 0.85-1.8V		1200		KHZ
Current Limit						
I_{CCLIM_BUS}	Bus average current Limit, V_{CSP2}- V_{CSN2}	Discharging mode		40		mV
		Charging mode		80		
NMOS Driver						
I_{HDRV}(Note 4)	Driver peak source current	VBST-VSW=6.6V		2		A
	Driver peak sink current	VBST-VSW=6.6V		2		A
I_{LDRV}(Note 4)	Driver peak source current	VCC=6.6V		2		A
	Driver peak sink current	VCC=6.6V		2		A
V_{BSTUV}	UVLO			2		V
	UVLO Hysteresis			300		mV
Output Protection						
V_{OVP}	Output over voltage threshold			110		%
V_{UVP}	Output under voltage threshold			50		%
VADJ, IADJ						
V_{TH_VADJ}(Note 4)	VPWM low voltage				0.4	V
	VPWM high voltage		2.5			V
V_{TH_IADJ}(Note 4)	IPWM low voltage				0.4	V

	IPWM high voltage		2.5	V
T_{SD} (Note 4)	Thermal Shutdown Threshold		150	°C
T_{HYS} (Note 4)	Thermal Shutdown Hysteresis		20	°C

Notes:
4) Guaranteed by design.

8 Typical Characteristics

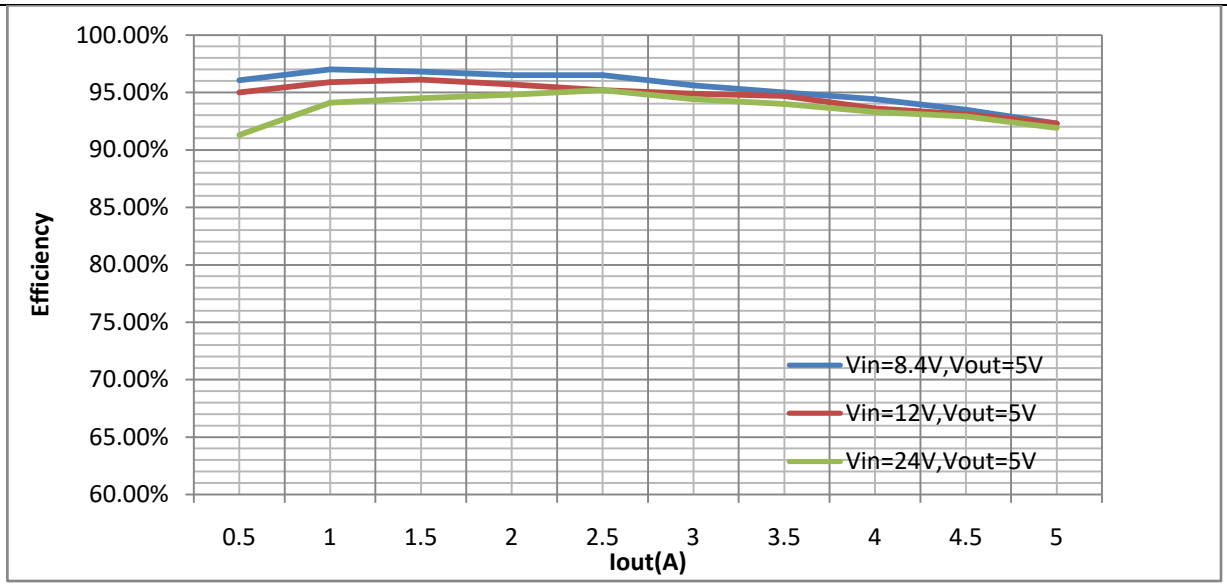
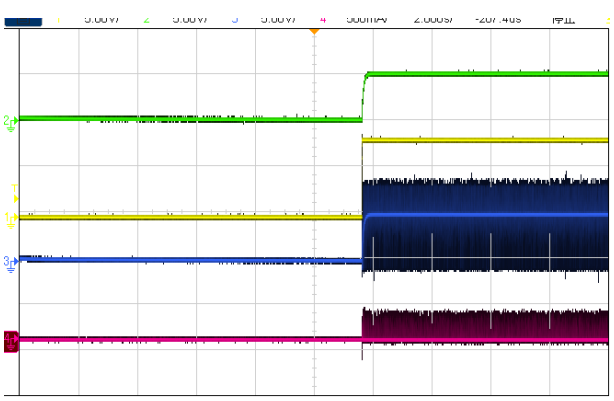


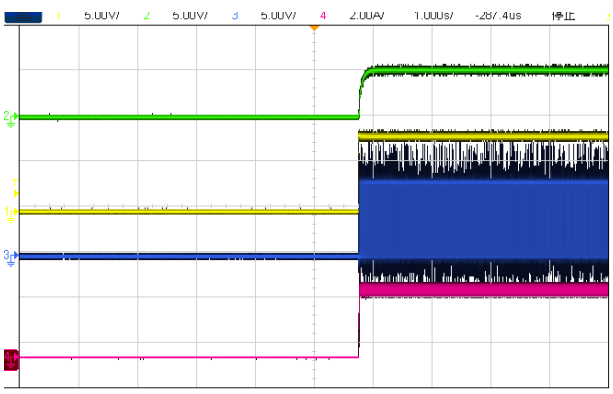
Fig. 3 Efficiency



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=8.4V Vout=5V

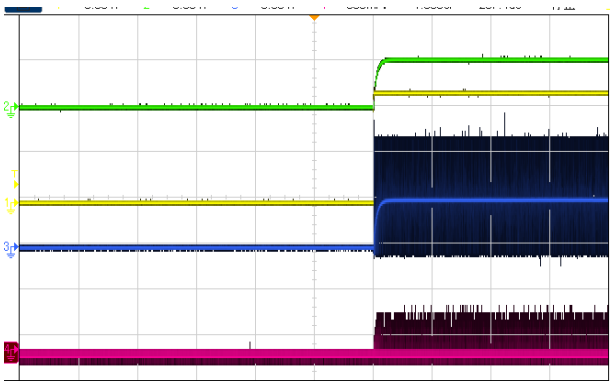
Fig.4 Start up waveform, Iout =0A



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=8.4V Vout=5V

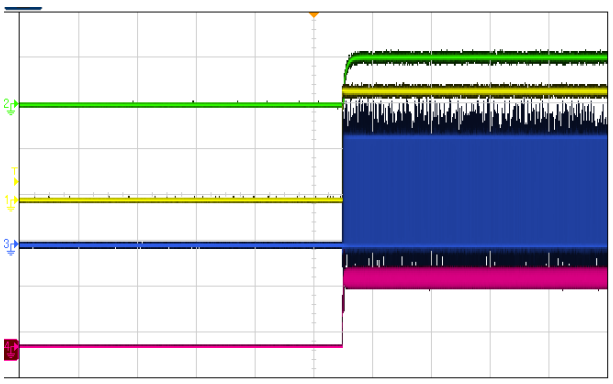
Fig.5 Start up waveform, Iout =3A



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=12V Vout=5V

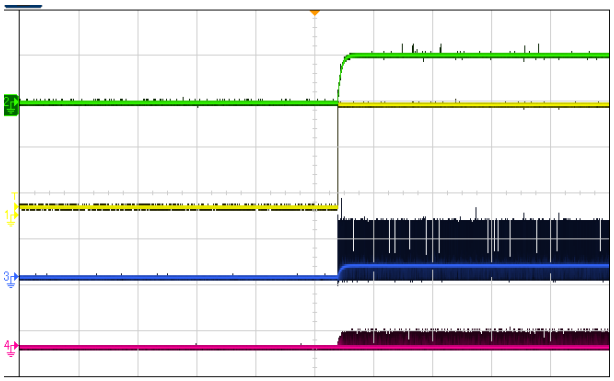
Fig.6 Start up waveform, Iout =0A



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=12V Vout=5V

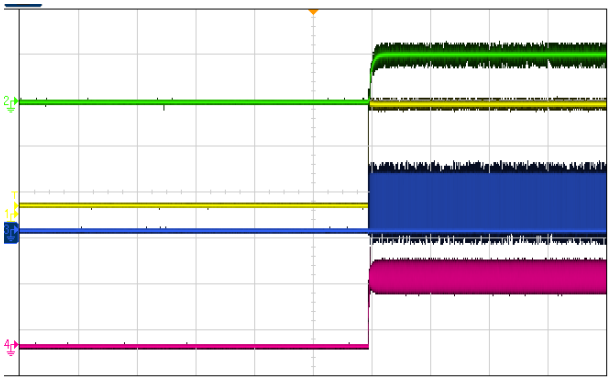
Fig.7 Start up waveform, Iout =3A



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=24V Vout=5V

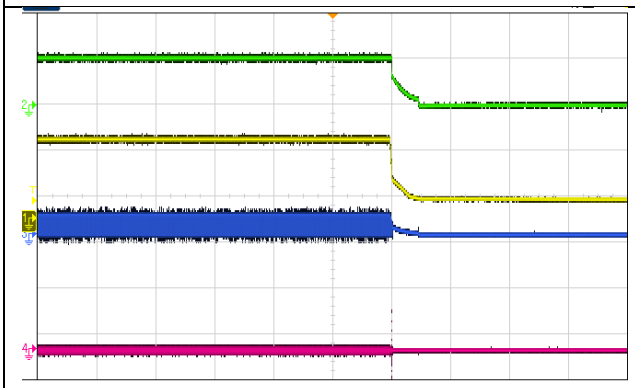
Fig.8 Start up waveform, Iout =0A



CH1: SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=24V Vout=5V

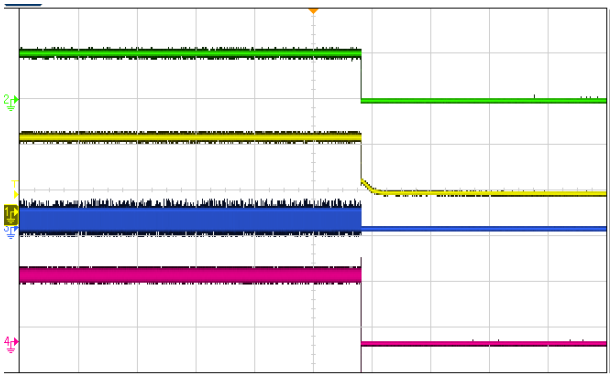
Fig.9 Start up waveform, Iout =3A



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=8.4V Vout=5V

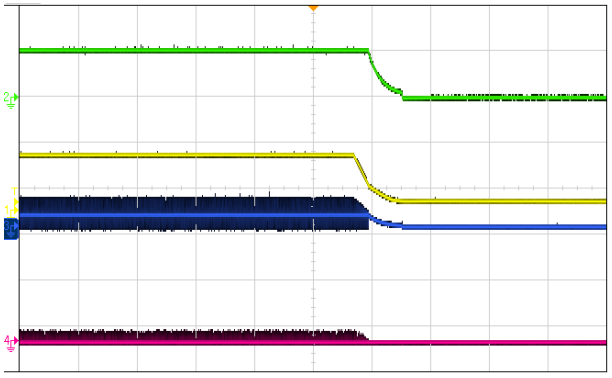
Fig.10 Shut down waveform, Iout =0A



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=8.4V Vout=5V

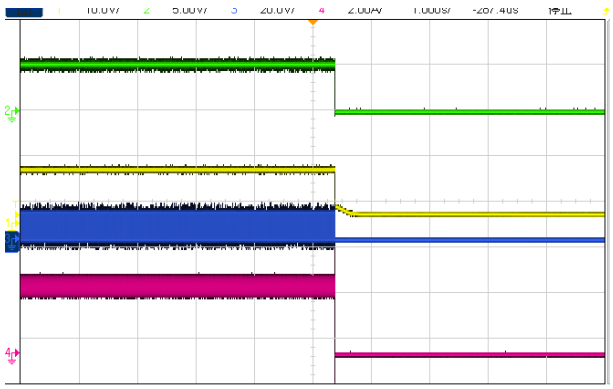
Fig.11 Shut down waveform, Iout =3A



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=12V Vout=5V

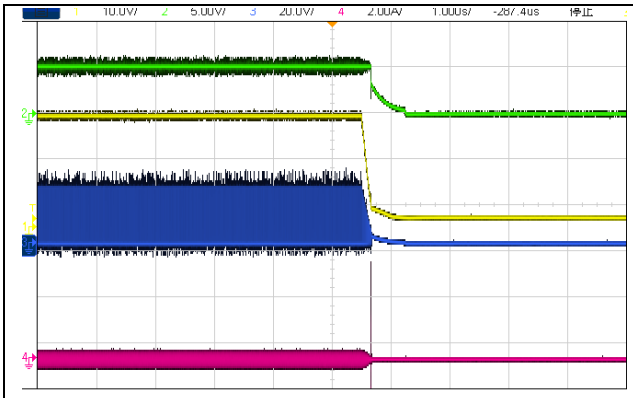
Fig.12 Shut down waveform, Iout =0A



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=12V Vout=5V

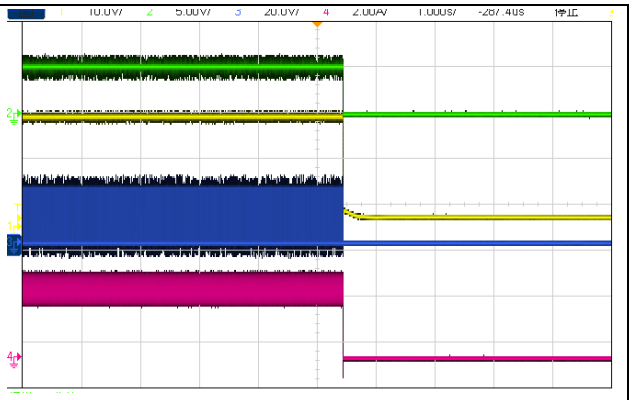
Fig.13 Shut down waveform, Iout =3A



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=24V Vout=5V

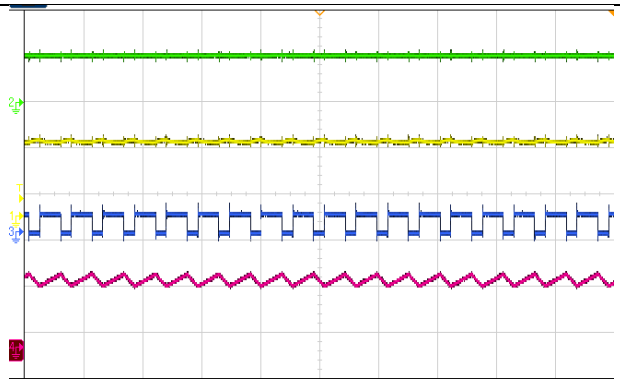
Fig.14 Shut down waveform, Iout =0A



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=24V Vout=5V

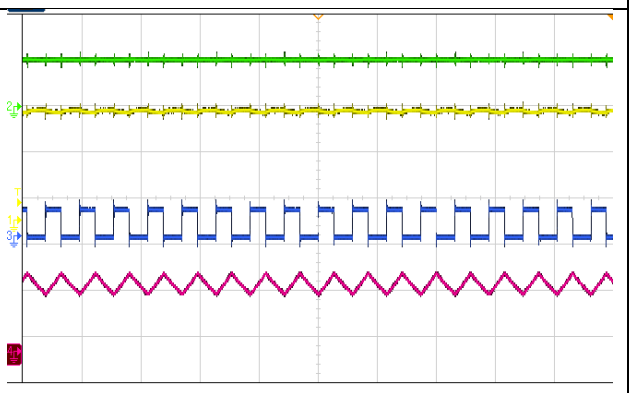
Fig.15 Shut down waveform, Iout =3A



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=8.4V Vout=5V

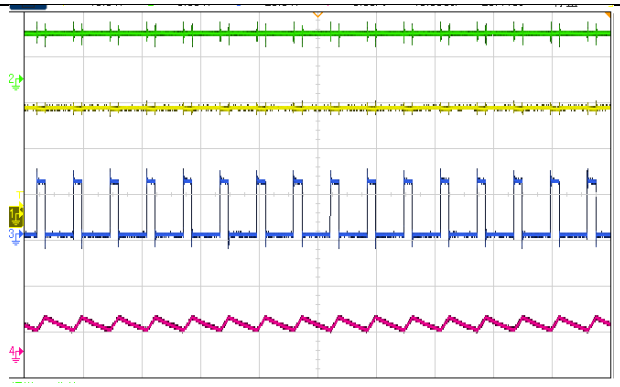
Fig.16 Steady State, Iout =3A



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=12V Vout=5V

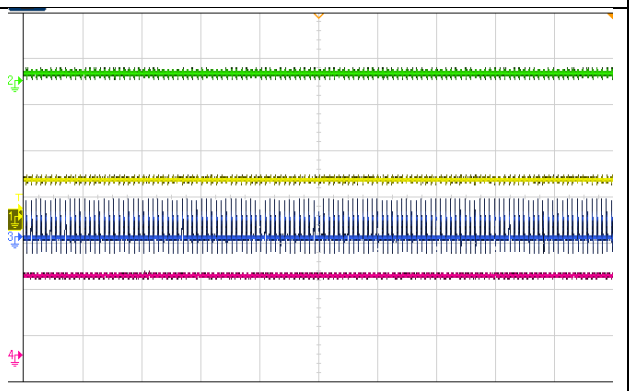
Fig.17 Steady State, Iout =3A



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=24V Vout=5V

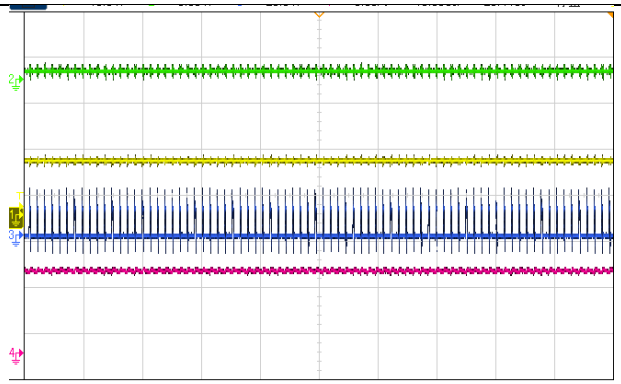
Fig.18 Steady State, Iout =3A



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=8.4V Vout=5V

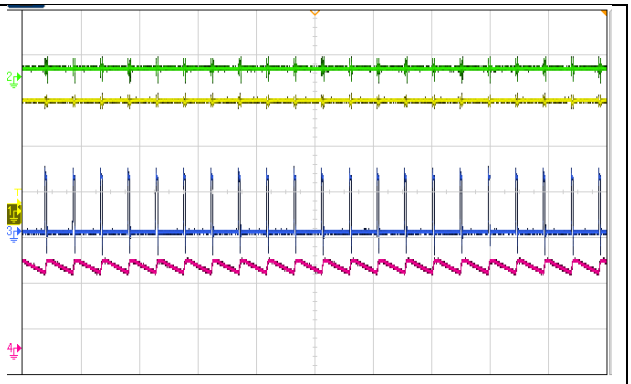
Fig.19 Short Circuit waveform



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=12V Vout=5V

Fig.20 Short Circuit waveform



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=24V Vout=5V

Fig.21 Short Circuit waveform

9 Detailed Descriptions

9.1 Overview

PL56001 is a PWM controller, designed for high performance synchronous Buck DC/DC applications with input voltages 4.5 V to 32 V (36 V maximum).

PL56001 employs Constant ON time control. The switching frequency could be set to 150kHz, 300kHz, 600kHz or 1200kHz based on different resistor value between FREQ pin and GND pin. The device also features a programmable soft-start function and offers all kinds of protection features including cycle-by-cycle current limiting, input under voltage lockout (UVLO), output over voltage protection (OVP), input Over Voltage Protection, thermal shutdown and output short protection etc.

9.2 Functional Block Diagram

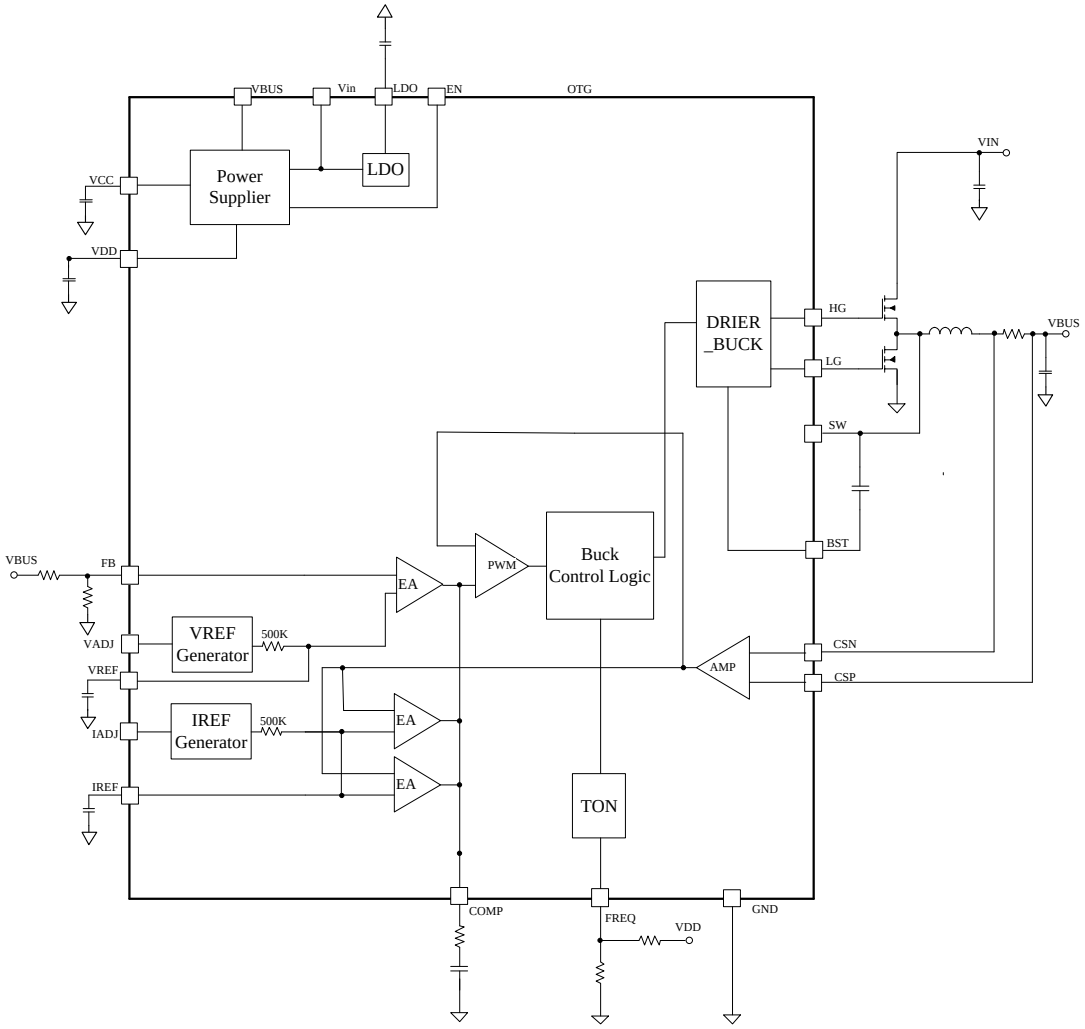


Fig. 22 PL56001 Block Diagram

9.3 Enable/UVLO

When EN is greater than 1.2V operating threshold, the control loop starts to work and regulate output to target voltage. When EN pin is below the standby threshold (1.1V typical), PL56001 stops working with only LDO is active to power MCU. EN is pulled high to 4V internally using a 2Meg resistor.

9.4 Over current Protection and short circuit protection

PL56001 provides cycle-by-cycle current limit to protect against over current and short circuit conditions. When VOUT is drop to UV threshold, PL56001 will go into hiccup mode to lower down power consumption.

9.5 Average Output Current Limiting

PL56001 provides optional average current limiting capability to limit either the output current. The average current limiting circuit uses an additional current sense resistor connected in series with the input supply or output voltage of the converter. A current sense gm amplifier with inputs at the CSP and CSN pins monitors the voltage across the sensing resistor and compares it with an internal 40 mV reference. If the drop across the sense resistor is greater than 40 mV, the gm amplifier regulates COMP voltage to lower down input or output current. The target constant current is given by Equation 1:

$$I_{CL(AVG)} = \frac{40\ mV}{R_{SNS}} \quad (1)$$

The average current loop can be disabled by shorting CSP to CSN.

9.6 Frequency Setting (FREQ) and frequency dithering

PL56001 switching frequency can be programmed at 150 kHz, 300 kHz or 600 kHz and 1200 kHz by voltage at FREQ pin to GND. When FREQ is connected to AGND, the switching frequency is set at 150 kHz. When FREQ is connected to VDD, the switching frequency is set at 300 kHz. A voltage divider between VDD and GND pin can be used to program switching frequency if 600 kHz or 1200 kHz is required.

9.7 Integrated Gate Drivers

PL56001 provides two N-channel MOSFET gate drivers: high-side gate drivers at the HG pin, and low-side drivers at the LG pin. Each driver is capable of sourcing 2 A and sinking 2 A peak current.

9.8 Thermal Shutdown

PL56001 is protected by a thermal shutdown circuit that shuts down the device when the internal junction temperature exceeds 160°C (typical). The soft-start capacitor is discharged when thermal shutdown is triggered and the gate drivers are disabled. The converter automatically restarts when the junction temperature drops by the thermal shutdown hysteresis of 15°C below the thermal shutdown threshold.

9.9 VREF and IREF

VREF pin is the final reference voltage used in the voltage regulation loop. When VADJ is connected to VDD, VREF will be 2V in discharging mode and 1.8V in charging mode. When VADJ is connected to a PWM signal, PWM signal will first be chopped to 2V and filter out using an internal resistor and external capacitor on VREF pin. The capacitor on VREF pin is also acting as soft-start capacitor at power up or in output voltage transition period. It is recommend using a relatively large capacitor such as 470nF for VREF pin and IREF pin.

The same mechanism works for IADJ and IREF pin.

10 Applications and Implementation

The typical application on the first page is a basic PL56001 application circuit. External component selection is driven by the load requirement, and begins with the selection of RS1, RS2 and the inductor value. Next, the power MOSFETs need to be selected. Finally, C_{IN} and C_{OUT} are selected. This circuit can be configured for operation up to an input voltage of 32V.

10.1 R_{CS} Selection

As shown in Figures 23, output current sense resistor RCS should be placed between the bulk capacitor for VBUS and the decoupling capacitor. A low pass filter formed by RF and CF is recommended to reduce the switching noise and stabilize the current loop. If output current limit is not desired, then CSP/CSN pins should be shorted to either VBUS.Place CSP/CSN symmetrically and keep them away switching signals such as BST SW, VIN, VBUS etc.

10.2 Inductor Selection

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. The inductor value has a direct effect on ripple current. The inductor current ripple ΔI_L is typically set to 20% to 40% of the maximum inductor current in the boost region at $V_{IN(MIN)}$.

For a given ripple, the inductance terms in continuous mode are as follows:

$$L>\frac{V_{OUT}*(V_{IN(MAX)}-V_{OUT})*1000}{f*\Delta I_L*V_{IN(MAX)}}\ uH \quad (2)$$

where: f is operating frequency, kHz

$V_{IN(MIN)}$ is minimum input voltage, V

$V_{IN(MAX)}$ is maximum input voltage, V

V_{OUT} is output voltage, V

ΔI_L is maximum inductor ripple current, A, usually select 20~40% maximum output current.

For high efficiency, choose an inductor with low core loss, such as ferrite. Also, the inductor should have low DC resistance to reduce the I2R losses, and must be able to handle the peak inductor current without saturating. To minimize radiated noise, use a toroid, pot core or shielded bobbin inductor.

10.3 C_{IN} and C_{OUT} Selection

Input capacitor C_{IN} is driven by the need to filter the input square wave current. Use a low ESR capacitor sized to handle the maximum RMS current, input RMS current is given by:

$$I_{CIN}=I_{OUT(MAX)}\times\sqrt{\frac{V_{OUT}}{V_{IN}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)} \quad (3)$$

This input current has a maximum at $V_{IN} = 2V_{OUT}$, $I_{CIN(MAX)} = I_{OUT(MAX)}/2$.

The effects of ESR (equivalent series resistance) and the bulk capacitance must be considered when choosing the right capacitor for a given output ripple voltage.

V_{OUT} ripple is given by:

$$\Delta V_{OUT}\leq\Delta I_L*\left(ESR+\frac{1}{8*f*C_{OUT}}\right) \quad (4)$$

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements.

10.4 Power MOSFET Selection and Efficiency Considerations

PL56001 requires two external N-channel power MOSFETs, the top switches Q1 and the bottom switches Q2. Important parameters for the power MOSFETs are the breakdown voltage $V_{BR, DSS}$, threshold voltage $V_{GS,TH}$, on-resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS} and maximum current $I_{DS(MAX)}$. The drive voltage is set by the 6.6V VCC supply to make the MOSFET's selection more flexible.

10.5 Output voltage setting

The PL56001 output voltage is set by an external feedback resistive divider carefully placed across the output capacitor. The 1% resistance accuracy of this resistor divider is preferred. The resultant feedback signal is compared with the

internal precision 2V voltage reference by the error amplifier. The output voltage is given by the equation:

$$V_{OUT} = 2V * \left(1 + \frac{R_1}{R_2}\right) \quad (5)$$

Where R_1 is the upper resistor and R_2 is the lower resistor in the feedback network.

11 PCB Layout

11.1 Guideline

Layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

1. The feedback network, resistor R1 and R2, should be kept close to the FB pin. Keep VBUS sensing path away from noisy nodes and preferably through a layer on the other side of shielding layer.
2. The input /output bypass capacitor must be placed as close as possible to the VIN/VBUS pin and ground. Grounding for both the input and output capacitors should consist of localized top side planes that connect to the GND pin and PAD. It is a good practice to place a ceramic cap near the VIN and VBUS pin to reduce the high frequency injection current.
3. Current sensing pairs (CSP,CSN) need to be placed carefully, Layout the lines symmetrically and keep them away from noisy nodes such as BST, SW, HG, LG etc. Connect these nodes directly to the two terminals of current sensing resistors Rcs1, Rcs2 to form an accurate Kelvin connection.

11.2 Application Examples

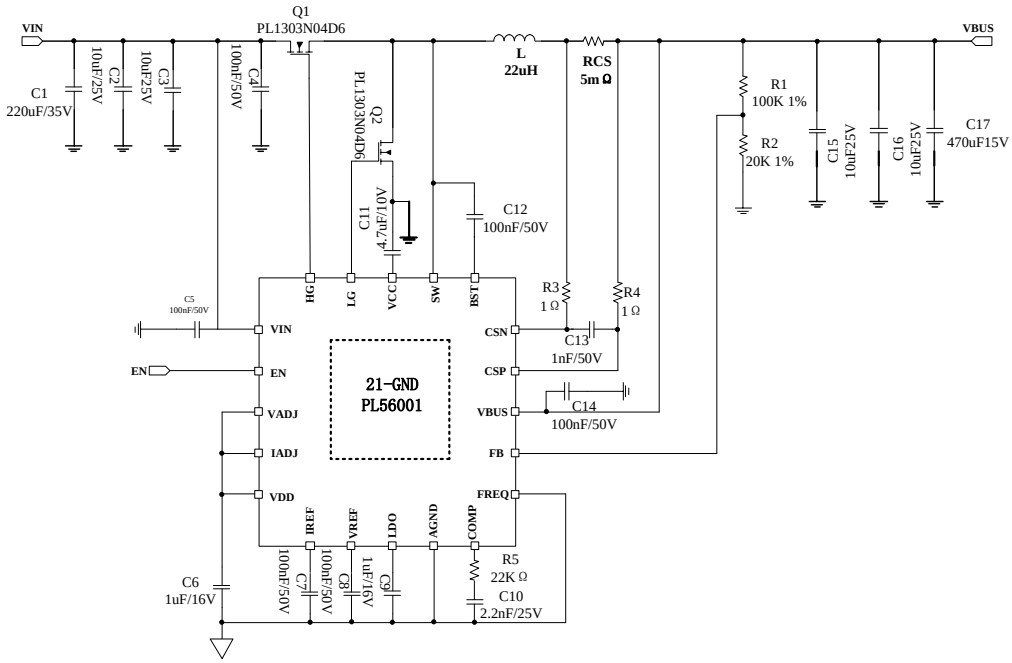


Fig. 23 Application Schematic (VABT:24V VBUS:12V IOUT:7A)

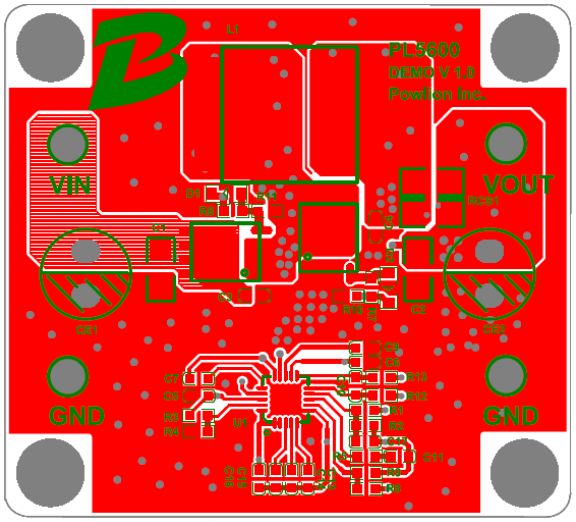


Fig. 24 Toplay

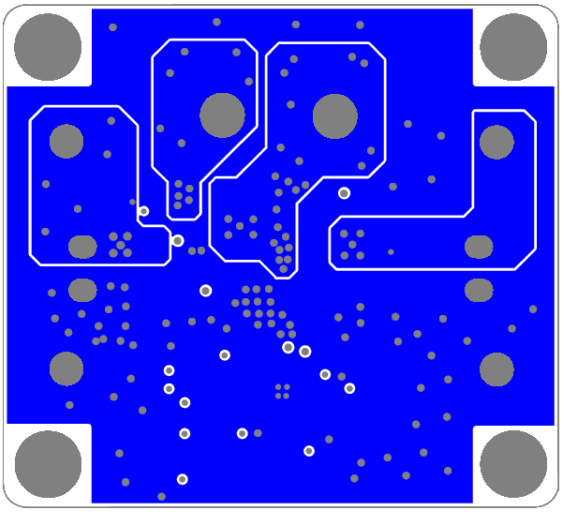
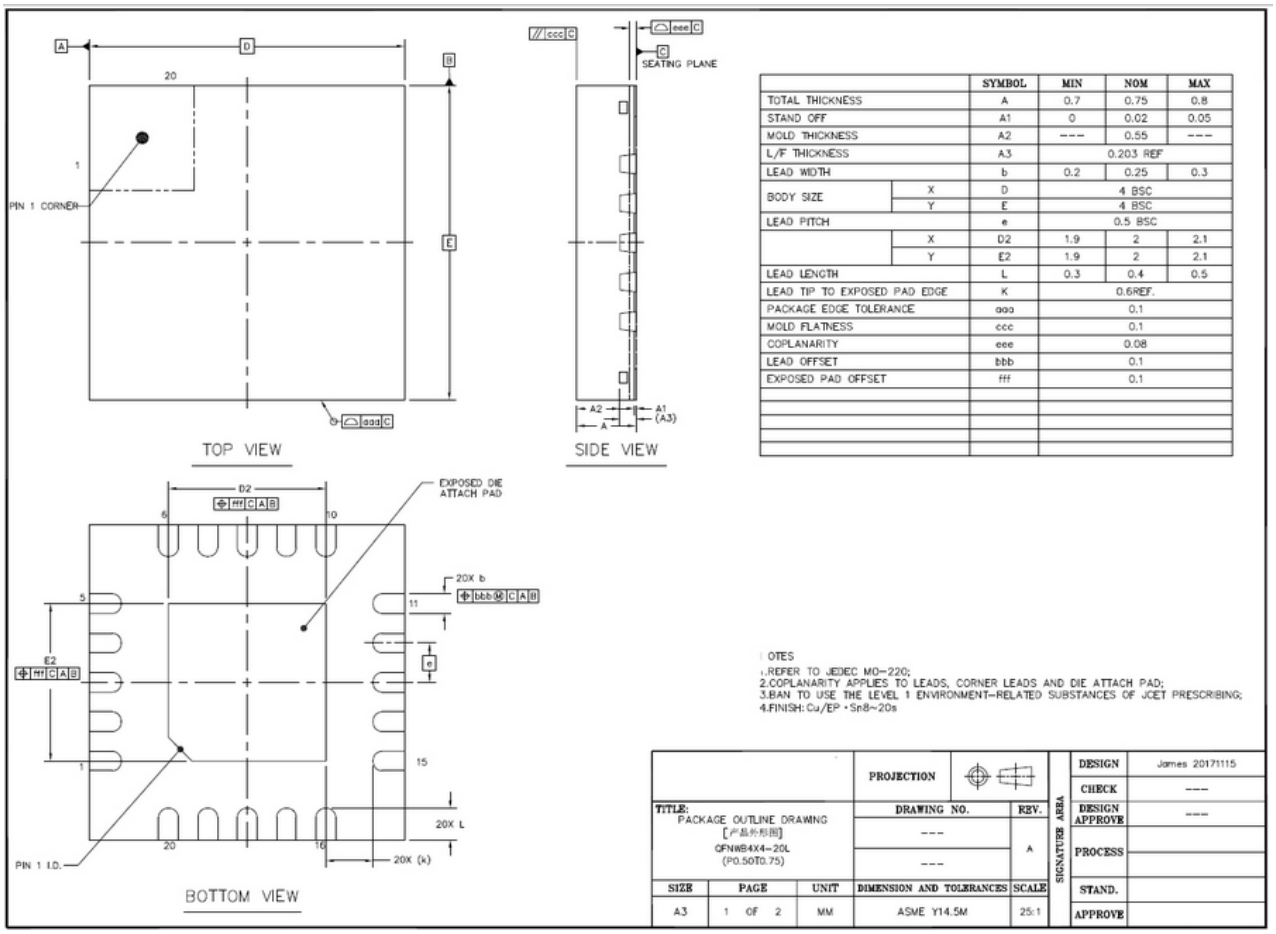


Fig. 25 Bottomlay

12 Packaging Information



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		4 BSC	
	Y	E		4 BSC	
LEAD PITCH		e		0.5 BSC	
	X	D2	1.9	2	2.1
	Y	E2	1.9	2	2.1
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.6REF.	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
EXPOSED PAD OFFSET		fff		0.1	

OTES
1.REFER TO JEDEC MO-220;
2.COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
3.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES OF JCET PRESCRIBING;
4.FINISH: Cu/EP · Sn8~20s

		PROJECTION			SIGNATURE AREA	DESIGN: James 20171115
TITLE: PACKAGE OUTLINE DRAWING [产品外形图] QFNWB4X4-20L (P0.50T0.75)		DRAWING NO.		REV.		CHECK: ---
		---		A		DESIGN APPROVE: ---
		---				PROCESS:
SIZE	PAGE	UNIT	DIMENSION AND TOLERANCES	SCALE		STAND.:
A3	1 OF 2	MM	ASME Y14.5M	25:1		APPROVE: